AMENDMENTS TO THE CLAIMS:

Applicant proposes to amend claim 10 and cancel claim 19. Claims 11-13 and 16 have been previously canceled and claims 1-9, 17 and 20 have been previously withdrawn. Upon entry of this Response by the Examiner, this listing of claims will replace all prior versions and listings of claims in the application.

1. (Withdrawn) A semiconductor device, comprising:

a gate oxide located over a substrate; and

a silicided gate electrode located over said gate oxide, said silicided gate electrode including a first metal and a second metal.

2. (Withdrawn) The semiconductor device as recited in claim 1 further including a dopant located within and configured to tune a work function of said silicided gate electrode.

3. (Withdrawn) The semiconductor device as recited in claim 2 wherein said dopant is selected from a group consisting of:

boron;

phosphorous; and

arsenic.

4. (Withdrawn) The semiconductor device as recited in claim 1 further including source/drain regions located in said substrate proximate said gate oxide and silicided

source/drain contact regions located in said source/drain regions, wherein said silicided source/drain contact regions have a depth substantially different than a thickness of said silicided gate electrode.

5. (Withdrawn) The semiconductor device as recited in claim 4 wherein said silicided gate electrode is silicided with a different metal than said silicided source/drain contact regions.

6. (Withdrawn) The semiconductor device as recited in claim 1 wherein said first metal is cobalt and said second metal is nickel.

7. (Withdrawn) The semiconductor device as recited in claim 6 wherein a ratio of an atomic percent of said cobalt to said nickel in said silicided gate electrode ranges from about 9:1 to about 2:3.

8. (Withdrawn) The semiconductor device as recited in claim 7 wherein said atomic percent ranges from about 3:1 to about 1:1.

9. (Withdrawn) The semiconductor device as recited in claim 1 wherein said silicided gate electrode has a thickness ranging from about 15 nm to about 150 nm.

10. (Currently Amended) A method for manufacturing a semiconductor device, comprising:

placing a layer of gate oxide material over a substrate;

forming a layer of silicided gate electrode material over said gate oxide, comprising:

forming a layer of polysilicon material over said layer of gate oxide material,

forming a layer of an alloy comprising a first metal and a second metal over said layer of polysilicon material, and

annealing said layer of said alloy comprising said first metal and said second metal to [[from]] form a layer of silicided gate electrode material including said first metal and said second metal; [[and]]

patterning said layer of silicided gate electrode material to form a silicided gate electrode; and

forming source/drain regions in said substrate and forming silicided source/drain contact regions in said source/drain regions subsequent to forming said silicided gate electrode.

11. – 13. (Canceled)

14. (Previously Presented) The method as recited in claim 23 further including forming a capping layer over said layer of said alloy, said capping layer configured to affect a doping profile of said dopant.

15. (Original) The method as recited in claim 14 wherein said capping layer comprises a transition metal-nitride.

16. (Canceled)

17. (Withdrawn) The method as recited in claim 11 wherein said cobalt-nickel alloy has a Co_x to Ni_y ratio (x:y) ranging from about 9:1 to about 2:3.

18. (Previously Presented) The method as recited in claim 10 wherein a ratio of an atomic percent of said first metal to said second metal in said silicided gate electrode ranges from about 9:1 to about 2:3.

19. (Canceled).

20. (Withdrawn) An integrated circuit, comprising:

transistors located over a substrate, said transistors including;

a gate oxide located over said substrate;

a silicided gate electrode located over said gate oxide, said silicided gate electrode including a first metal and a second metal; and

an interlevel dielectric layer located over said substrate, said interlevel dielectric layer having interconnects located therein for contacting said transistors.

21. (Previously Presented) The method as recited in claim 18 wherein said first metal is cobalt and said second metal is nickel.

22. (Previously Presented) The method as recited in claim 10 wherein said first metal is cobalt and said second metal is nickel.

23. (Previously Presented) The method of claim 10, further comprising:

implanting a dopant into said layer of polysilicon material affecting a work function of said silicided gate electrode.

24. (Previously Presented) The method of claim 10, wherein a ratio of a thickness of the layer of polysilicon material to a thickness of the layer of the alloy is at least approximately 3.6:1.